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EXAMINER	
RUTLAND WALLIS, MICHAEL	
ART UNIT	**PAPER NUMBER**
2835	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/603,837	CHUANG, YING-LANG	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2835	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are: paragraph 0016 a first count line 1, a second count line 2, a third count line 3, paragraph 0042 lines 1-2 "According to the present invention, the signal bounce can be inhibited by properly toggling some of the signals on simultaneously changing" it is not clear to the office what is being changed.

Claim Objections

Claim 3 is objected to because of the following informalities: lines 2-3 states "and remains said second internal signal unchanged" should be changed to read "that remains unchanged".

Claims 4-5, 9-10, 13 and 18 are objected to as the use of the word "count" as it is unclear. It is suggested by the examiner to be changed to read "a plurality".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-5, 9, 11-13 and 16-18 are rejected under 35 U.S.C. 102(a) as being anticipated by Bonaccio et al. (U.S. Pat. No. 6,345,380).

With respect to claim 1 Bonaccio teaches a signal bounce inhibiting device (Fig. 1 or 2) for preventing from power/ground bounce, comprising: an electric level toggling circuit (Fig. 2 item 24) receiving a first internal signal of a first chip (Fig. 2 item 10), and toggling said first internal signal into a first output signal in response to a first toggling control signal inputted therein; and an electric level recovering circuit (Fig. 2 item 25 and Fig. 1 90 and 91) receiving said first output signal, and recovering said first output signal into said first internal signal required by a second chip (Fig. 2 item 11) in response to a first recovering control signal inputted therein.

With respect to claim 2 Bonaccio teaches said electric level toggling circuit (Fig. 2 item 24) is disposed in an output stage of said first chip and said electric level recovering circuit (Fig. 2 item 25 and Fig. 1 90 and 91) is disposed in an input stage of said second chip (see figure 2 for teaching of circuit location on the chip).

With respect to claim 3 Bonaccio teaches said electric level toggling circuit further receives a second internal signal (Bonaccio teaches signals are sent through communication buses 32 33 and 34) and said second internal signal (Bonaccio teaches signals are sent through communication buses 32 33 and 34) remains unchanged as a second output signal in response to a second toggling control signal inputted therein, and said electrical level recovering circuit and said second output signal remain unchanged in response to a second recovering control signal inputted therein so as to provide said second internal signal for said second chip (Bonaccio teaches signals carried through I/O circuit 28 to I/O circuit 29 remain unchanged see column 6 line 61 – column 7 line 22).

With respect to claims 4 and 13 Bonaccio teaches said electric level toggling circuit includes a first count (Fig. 2 items 26a 24a and 28a which control the sending of signals further in column 4 lines 1-5 Bonaccio teaches there may be hundreds or thousands of the chips containing these circuits) of electric level toggling units for toggling a second count (Bonaccio teaches signals are sent through communication buses 32 33 and 34) of said first internal signals into said first output signals in response to said second count of first toggling control signals (Bonaccio teaches toggling control signals are received from functional circuitry see column 4 lines 47-59), and remaining a third count of said second internal signals (Bonaccio teaches signals are sent through communication buses 32 33 and 34) into said second output signals in response to said third count of second toggling control signals.

With respect to claim 5 Bonaccio teaches said electric level recovering circuit includes said first count of electric level recovering units (Fig. 2 item 25, 27 and 29 and Fig. 1 90 and 91) for recovering said second count of said first output signals into said first internal signals in response to said second count of said first recovering control signals, and remaining said third count of said second output signals into said second internal signals in response to said third count of said second recovering control signals.

With respect to claim 9 Bonaccio teaches a method for providing internal signals from a first chip to a second chip with inhibited power/ground bounce (see Fig. 1 or 2), comprising steps of: asserting a plurality of toggling control signals (Bonaccio teaches toggling control signals are received from functional circuitry see column 4 lines 47-59) including a first count of first toggling control signals and a second count (Fig. 2 see functional circuitry item 12 connecting to I/O circuits 24a 26a and 28a for sending signals through communication buses items 32, 33 and 34) of second toggling control signals; toggling said first count of said internal signals into said first count of output signals in response to said first count of said first toggling control signals, and remaining said second count of said internal signals unchanged (Bonaccio teaches signals carried through I/O circuit 28 to I/O circuit 29 remain unchanged see column 6 line 61 – column 7 line 22) in response to said second count of said second toggling control signals; asserting a plurality (Fig. 2 items 26a 24a and 28a which control the sending of signals further in column 4 lines 1-5 Bonaccio teaches there may be hundreds or thousands of the chips containing these circuits) of recovering control signals (Fig. 2 item 91) correlating to said plurality of toggling control signals, and including said first count of

first recovering control signals and said second count of second recovering control signals; and recovering (Bonaccio teaches receiving signals through communication buses items 32, 33 and 34) said first count of said output signals into said first count of said internal signals in response to said first count of said first recovering control signals, and remaining said second count of said internal signals unchanged in response to said second count of said second recovering control signals.

With respect to claim 11 Bonaccio teaches said first toggling control signal and said first recovering control signal are both at high levels (column 5 lines 49-65), and said second toggling control signal and said second recovering control signal are both at low levels (Bonaccio teaches the use of Pets connected to high voltage Vdd and second control voltages NFETs connected to ground see FETs 48 and 49 for example).

With respect to claim 12 Bonaccio teaches a signal bounce inhibiting device (Fig. 1 or 2) embedded in an integrated chip for preventing signals from power/ground bounce, comprising: an electric level toggling circuit (Fig. 2 item 24) toggling a first internal signal into a first output signal in response to a first toggling control signal (Bonaccio teaches toggling control signals are received from functional circuitry see column 4 lines 47-59) and remaining a second internal signal unchanged (Bonaccio teaches signals carried through I/O circuit 28 to I/O circuit 29 remain unchanged see column 6 line 61 – column 7 line 22) as a second output signal in response to a second toggling control signal; and a storing device (Figs. 4 and 7 item 80 and 81 further the processor is understood to contain additional storing memory) for storing said first toggling control signal and said second toggling control signal.

With respect to claim 16 Bonaccio teaches an electric level recovering circuit (Fig. 2 item 25 and Fig. 1 90 and 91) disposed in a target chip (item 11) for receiving and recovering said first output signal into said first internal signal in response to a first recovering control signal inputted therein.

With respect to claim 17 Bonaccio teaches said electric level recovering circuit remains said second output signal unchanged (Bonaccio teaches signals carried through I/O circuit 28 to I/O circuit 29 remain unchanged see column 6 line 61 – column 7 line 22) in response to a second recovering control signal so as to provide said second internal signal for said target chip (Bonaccio teaches item 91 protects the circuit from voltage bounce but does not alter the signal).

With respect to claim 18 Bonaccio teaches said electric level recovering circuit includes a first count (Fig. 2 item 25 and Fig. 1 90 and 91 Bonaccio teaches there may be hundreds or thousands of the chips containing these circuits) of electric level recovering units (Fig. 2 item 25, 27 and 29 and Fig. 1 90 and 91) for recovering a second count of said first output signals (Fig. 2 item 25 27 and 29 receive signals from their counter parts 24, 26 and 28) into said first internal signals in response to said second count of said first recovering control signals, and remaining said third count of said second output signals into said second internal signals in response to said third count of said second recovering control signals.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-8, 14, 15, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonaccio et al. (U.S. Pat. No. 6,345,380) in view of Chan et al (U.S. Pat. No. 6,294,925).

With respect to claims 6-7 Bonaccio teaches said electric level toggling circuit includes a plurality of electric level toggling units and recovery units and further uses OR gate logic in his design (items 82 and 83) and a latch for inputting therein and storing a certain toggling control signal, but does not teach the use of XOR gates for receiving said certain toggling control signal and a certain internal signal to perform a first XOR operation or a register for inputting therein and storing a certain toggling control signal, thereby toggling said certain internal signal or remaining said certain internal signal unchanged so as to obtain a certain output signal. Chan teaches a circuit which uses memory and delay system to reduce noise and ground bounce (column 8 lines 3-56). Chan's circuit uses a XOR gate (Chan Fig. 3 item 51) and register (Fig. 3 item 58) in his circuit (item 34). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Bonaccio to use a XOR gates instead of OR gates in order to control the output signal to be low when two high signals are inputted and a register as an alternative to a latch in order to store more information.

With respect to claim 8 Bonaccio teaches said first and said second toggling control signals come from functional circuitry to said first and said second recovering control signals. While Bonaccio is silent on what type of circuitry this is. It would have been obvious to one of ordinary skill in the art at the time of the invention to have this functional circuitry provide the same signal to two of the output circuits (items 26a and 28a) in order to have a redundant output circuit to provide redundancy and insure accuracy.

With respect to claim 14 Bonaccio teaches said electric level toggling circuit (Fig. 2 item 24) includes a plurality of electric level toggling units (Fig. 2 items 26a 24a and 28a which control the sending of signals further in column 4 lines 1-5 Bonaccio teaches there may be hundreds or thousands of the chips containing these circuits). Bonaccio does not teach the use of XOR gate in the reception of the toggling control signal. Chan's circuit uses a XOR gate (Chan Fig. 3 item 51 see column 9 lines 55-65) in his circuit (item 34). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Bonaccio to use a XOR gates instead of OR gates in order to control the output signal to be low when two high signals are inputted.

With respect to claim 15 Bonaccio teaches said storing device includes a plurality of storing units (Figs. 4 and 7 item 80 and 81 further the processor is understood to contain additional storing memory). Bonaccio does not teach the use of registers dedicated memory for each circuit. Chan teaches a circuit which uses memory to reduce noise and ground bounce (column 8 lines 3-56). Chan's circuit uses register type memory (Fig. 3 item 58) in his circuit (item 34). It would have been obvious to one of

ordinary skill in the art at the time of the invention to modify Bonaccio a register as an alternative to a latch memory in Bonaccio's current design in order to store more information.

With respect to claim 19 Bonaccio teaches said electric level toggling circuit includes a plurality of electric level toggling units (Fig. 2 items 26a 24a and 28a which control the sending of signals further in column 4 lines 1-5 Bonaccio teaches there may be hundreds or thousands of the chips containing these circuits). Bonaccio does not teach the use of XOR gates for receiving said certain toggling control signal and a certain internal signal to perform a first XOR operation thereby toggling said certain internal signal or remaining said certain internal signal unchanged so as to obtain a certain output signal. Chan teaches a circuit which uses memory and delay system to reduce noise and ground bounce (column 8 lines 3-56). Chan's circuit uses a XOR gate (Chan Fig. 3 item 51) and register (Fig. 3 item 58) in his circuit (item 34). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Bonaccio to use a XOR gates instead of OR gates in order to control the output signal to be low when two high signals are inputted.

With respect to claim 20 Bonaccio teaches said electric level toggling circuit includes a storing unit (Fig. 4 item 80), but Bonaccio does not teach plural storing circuits each containing a register for inputting therein and storing said first recovering control signal or said second recovering control signal. Chan's circuit utilizes register memory (Fig. 3 item 58) in his circuit (item 34). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Bonaccio to use a register

as an alternative to a latch in order to store more information to reduce signal bounce in each circuit.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bonaccio et al. (U.S. Pat. No. 6,345,380). Bonaccio teaches said first and said second toggling control signals come from functional circuitry to said first and said second recovering control signals. While Bonaccio is silent on what type of circuitry this is. It would have been obvious to one of ordinary skill in the art at the time of the invention to have this functional circuitry provide the same signal to two of the output circuits (items 26a and 28a) in order to have a redundant output circuit to provide redundancy and insure accuracy.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (U.S. Pat. No. 6,622,256) Dabral et al., (U.S. Pat. No. 6,043,682) Dabral et al., (U.S. Pat. No. 6,229,336) Felton et al., (U.S. Pub. No. 20030159096) Balzer, (U.S. Pat. No. 5,920,204) Bruno et al. (U.S. Pub. No. 20030042925) and Kirk (U.S. Pub. No. 20030042925) teaches a similar apparatus a method for reducing ground and/or voltage bounce.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-

272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn D. Feild can be reached on 571-272-2092. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MRW

ANATOLY VORTMAN
PRIMARY EXAMINER